SMMA001

TM4164EC4 Provides High-Density Memory Array

MOS Memory Products
Application Report

TEXAS INSTRUMENTS

IMPORTANT NOTICE

TM4164EC4 Provides High-Density Memory Array

MOS Memory
Applications Engineering

This Application Report illustrates the use of the TM4164EC4 (64K × 4) Memory Module with the TMS4500A DRAM Controller (see Figure 1). The description of a memory board using both devices will be given along with full schematics, edge connector pinout, and signal description. An interface to the Intel 8086 microprocessor is also provided as a typical application.

BOARD DESCRIPTION

Designed by Texas Instruments to demonstrate the TM4164EC4 in a system environment, the board provides a flexible, high-density memory array which is adaptable to most applications.

The board uses one TMS4500A and eight TM4164EC4s for 256K bytes of dynamic RAM memory on a 3.25 inch × 4.5 inch card. The TMS4500A gives the board a static appearance in the system, providing many of the necessary timing and control signals to the DRAM array. Each TM4164EC4 is comprised of four TMS4164 plasitic-leaded-chip-carriers and two ceramic chip capacitors, that are surface mounted on a PC substrate to form a single-in-line package (SIP).[1] The cost savings that can be realized with SIPs include reduced PC board size, fewer plated-through-holes, and the elimination of bypass capacitors on the motherboard.

The TM4164EC4 SIPs are mounted on 0.350 inch centers, and occupy 6.16 square inches of board area

[1]See Appendix A.

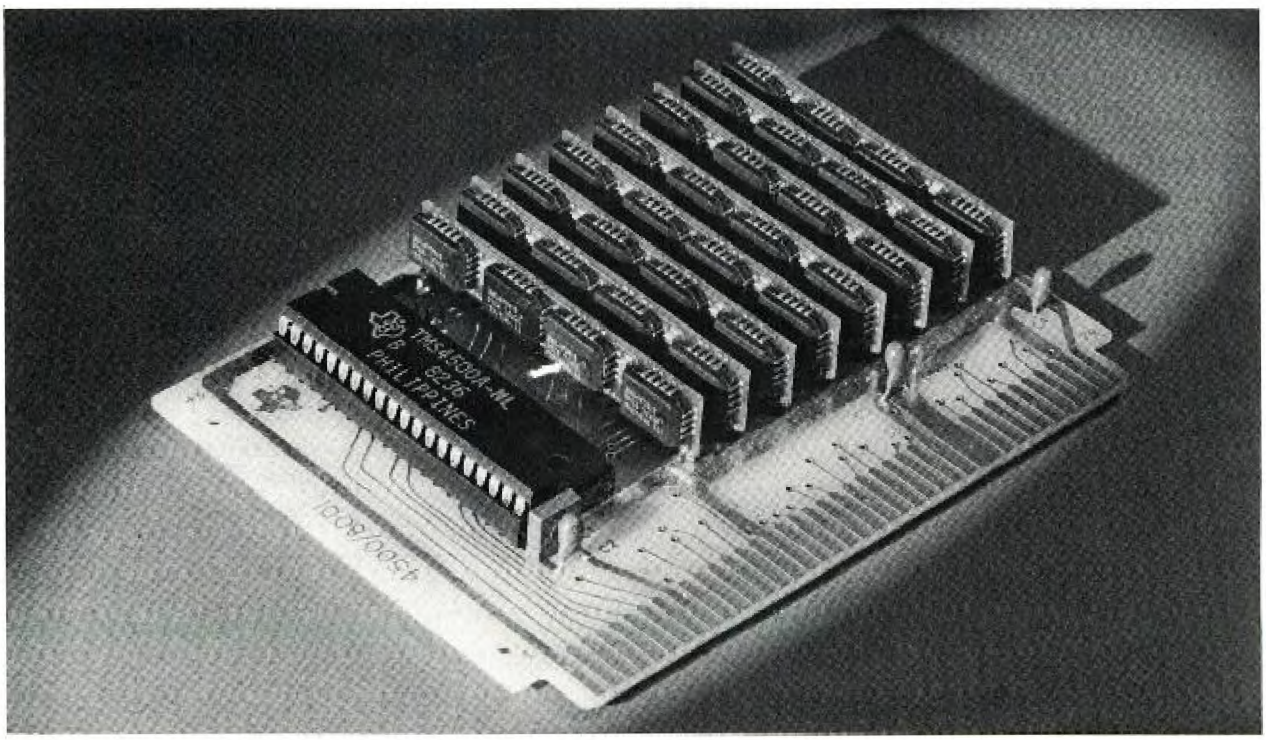

Figure 1. TM4164EC4/TMS4500A Memory Board

[8 × 0.350 × 2.2 inches (TM4164EC4 length)], for a density of greater than five memory devices per square inch. This is approximately a 2X density improvement with respect to DIPs. The TM4164EC4s can be mounted on centers as narrow as 0.200 inches if adequate cooling is provided. This would give a density of greater than nine memory devices per square inch or approximately a 3.5X improvement over DIPs for the above array.

The equivalent DIP implementation of the TM4164EC4 would require 68 plated-through-holes (four 16-pin packages and two, 2-lead capacitors) as opposed to the 22 required for a single TM4164EC4. The large number of plated-through-holes increase board cost and reduce the available PC board area for trace routing often requiring an increase in the number of board layers.

The on board capacitors eliminate the need for bypassing on the motherboard and offer superior performance over equivalent leaded capacitors due to the reduced lead inductance.

While the TMS4500A gives the board a static appearance and the TM4164EC4 provides a high-density memory array, the interconnect bus gives the board flexibility. All the signals necessary to provide for 8- or 16-bit operation, separate or common I/O, and internal or external memory refresh along with the address and control lines for the TMS4500A are brought to the board edge.

MEMORY ORGANIZATION

The memory is organized as two banks of 128K bytes, accessible in byte or word format (word = 16 bits). Each row is selected by $\overline{\text{RAS0}}$ or $\overline{\text{RAS1}}$ (see Figure 2) to provide 16 bits of available data. The 16 bits of data are then read or written in byte or word format by controlling the upper and lower $\overline{\text{CAS}}$ and $\overline{\text{WR}}$ signals ($\overline{\text{UCAS}}$, $\overline{\text{LCAS}}$, $\overline{\text{UWR}}$, and $\overline{\text{LWR}}$). The lower byte of data corresponds to D0-D7 and Q0-Q7, while upper data corresponds to D8-D15 and Q8-Q15. It is necessary to organize the memory as such to provide operation with 16-bit microprocessors that do both byte and word accesses. For microprocessors with 8-bit data busses, D0-D7 and Q0-Q7 are tied to D8-D15 and Q8-Q15, respectively. The $\overline{\text{CAS}}$ and $\overline{\text{WR}}$ signals are then used to multiplex and demultiplex the data onto and from the microprocessor data bus.

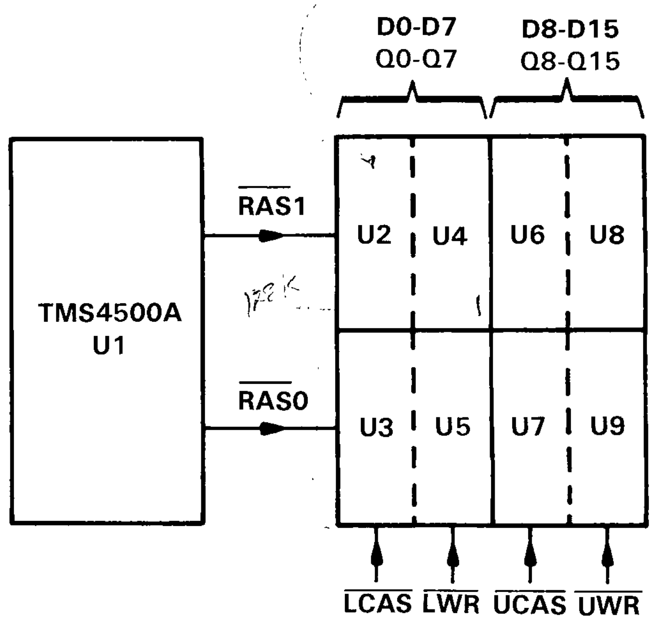

Figure 2. Block Diagram

Table I. Pin Nomenclature

Name	Description
A0-A15	Address Inputs
$\overline{\text{ACR}}$	Access Control, Read
$\overline{\text{ACW}}$	Access Control, Write
ALE	Address Latch Enable
$\overline{\text{BRDEN}}$	Board Enable
$\overline{\text{CAS}}$	Column Address Strobe
CLK	Clock Input
D0-D15	Data In
FS0	Frequency Select 0
FS1	Frequency Select 1
GND	Ground
$\overline{\text{LCAS}}$	Lower $\overline{\text{CAS}}$
$\overline{\text{LWR}}$	Lower Write
$\overline{\text{REFREQ}}$	Refresh Request
REN1	$\overline{\text{RAS}}$ Enable 1
RDY	Ready
Q0-Q15	Data Out
TWST	Timing/Wait Strap
$\overline{\text{UCAS}}$	Upper $\overline{\text{CAS}}$
$\overline{\text{UWR}}$	Upper Write
+5	+5 Volts

BOARD OPERATION

As mentioned earlier the board provides a 16-bit data bus with separate data-in and data-out connections (see Figure 3). This allows the board to be configured for common (D0-D15 tied to Q0-Q15) or separate input/output (I/O). Notice that corresponding D and Q lines are located across from each other for easy interconnection (see Table II). Common I/O operation requires the memory array to be accessed in the early-write mode ($\overline{\text{WR}}$ low prior to $\overline{\text{CAS}}$). The board provides flexible control of the memory array by bringing $\overline{\text{CAS}}$ from the TMS4500A to the board edge allowing it to be combined with external logic to derive the $\overline{\text{UCAS}}$ and $\overline{\text{LCAS}}$ signals. If desired the $\overline{\text{CAS}}$ signal from the TMS4500A can directly drive the memory array by connecting $\overline{\text{CAS}}$ to $\overline{\text{UCAS}}$ and $\overline{\text{LCAS}}$ via jumpers J1 and J2. This type of configuration necessitates the use of $\overline{\text{LWR}}$ and $\overline{\text{UWR}}$ to control access to the memory array on write cycles. Also, all 16 bits of data will be active on a read cycle for both byte and word accesses. All the necessary signals needed to interface to the TMS4500A have been brought to the board edge. Notice that the binary weighting on the memory address outputs of the TMS4500A do not correspond to that of the TM4164EC4 memory addresses. This does not in any way affect the operation of the board as the TM4164EC4s are random-access devices. This configuration was chosen to simplify the board layout. Table III gives the relationship between the TMS4500A and TM4164EC4 addresses.

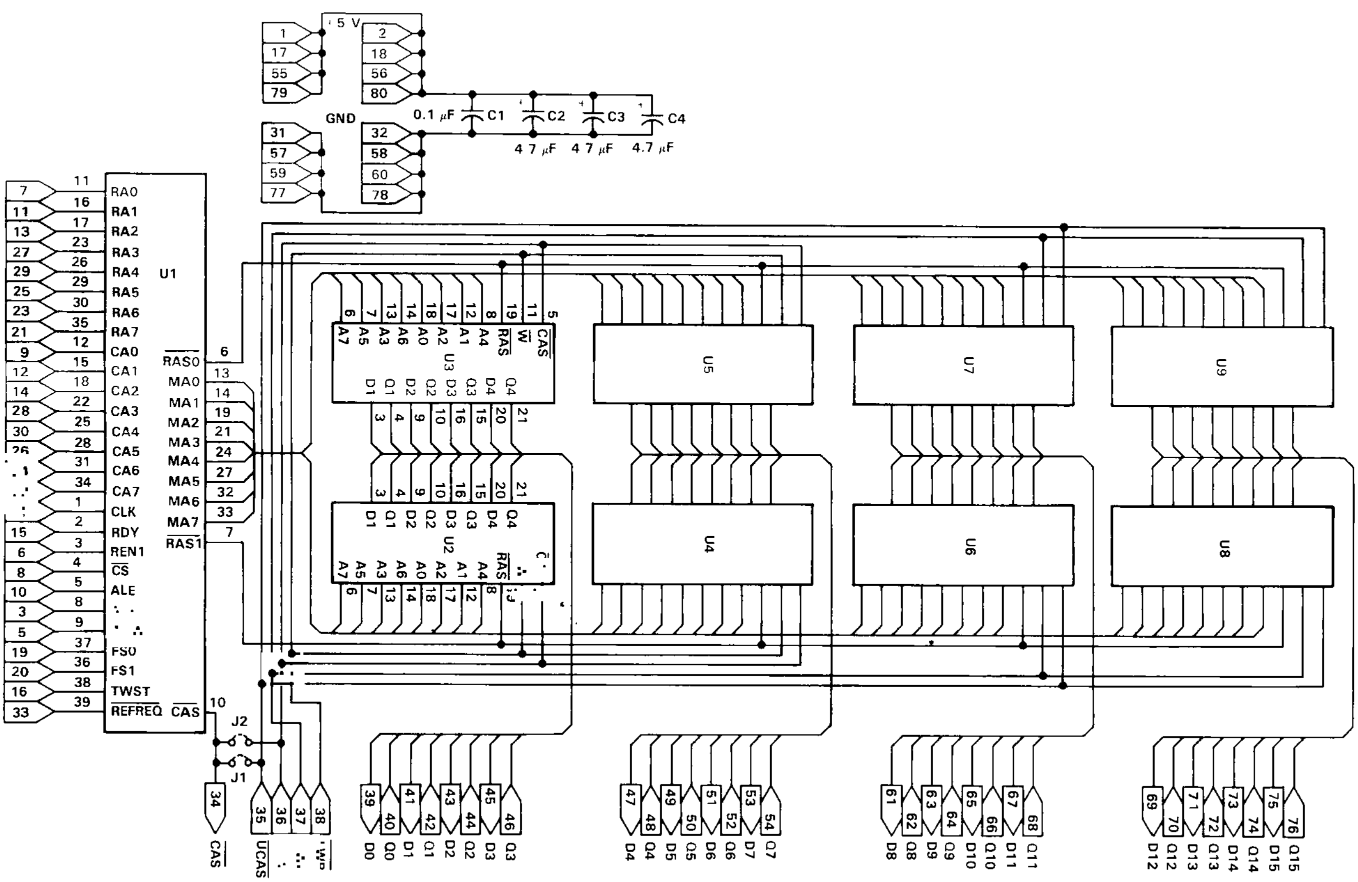

Figure 3. Board Schematic

Table II. Buss Format

Pin	Signal	Pin	Signal
1	+5	2	+5
3	$\overline{ACR}$	4	CLK
5	$\overline{ACW}$	6	REN1
7	A0	8	BRDEN
9	A8	10	ALE
11	A1	12	A9
13	A2	14	A10
15	RDY	16	TWST
17	+5	18	+5
19	FS0	20	FS1
21	A7	22	A15
23	A6	24	A14
25	A5	26	A13
27	A3	28	A11
29	A4	30	A12
31	GND	32	GND
33	$\overline{REFREQ}$	34	$\overline{CAS}$
35	$\overline{UCAS}$	36	$\overline{LCAS}$
37	$\overline{UWR}$	38	$\overline{LWR}$
39	D0	40	Q0
41	D1	42	Q1
43	D2	44	Q2
45	D3	46	Q3
47	D4	48	Q4
49	D5	50	Q5
51	D6	52	Q6
53	D7	54	Q7
55	+5	56	+5
57	GND	58	GND
59	GND	60	GND
61	D8	62	Q8
63	D9	64	Q9
65	D10	66	Q10
67	D11	68	Q11
69	D12	70	Q12
71	D13	72	Q13
73	D14	74	Q14
75	D15	76	Q15
77	GND	78	GND
79	+5	80	+5

Table III. Address Relationship

TMS4500A	TM4161EC4
MA0	A4
MA1	A1
MA2	A2
MA3	A0
MA4	A6
MA5	A3
MA6	A5
MA7	A7

8086 INTERFACE

The circuit is designed to operate with a 5 MHz 8086 in the maximum mode configuration without memory wait states (see Figure 4). The memory interface is simplified by configuring the memory for early write operation, which allows corresponding D and Q lines to be tied together for common I/O operation (see Table II). The board select logic is derived from addresses A18 and A19 and mapped via a 74S139 at address locations 40000-7FFFF hex (256K bytes). Address A17 is connected to REN1 of the TMS4500A to defferentiate between the two banks of memory (REN1 = 0, selects $\overline{RAS0}$; REN1 = 1, selects $\overline{RAS1}$). To provide for byte accesses, AD0 and $\overline{BHE}$ are combined with other logic to yield the necessary upper and lower $\overline{CAS}$ signals ($\overline{UCAS}$ and $\overline{LCAS}$). The 8284 is strapped for asynchronous ready operation to provide sufficient $\overline{CAS}$ access time on access-grant cycles. See the *TMS4500A Users Manual* for details of the TMS4500A operation. The $\overline{AMWC}$ and $\overline{MRDC}$ signals from the 8288 are used to derive $\overline{ALE}$ and $\overline{ACR}$ which initiates memory-access cycles. $\overline{AMWC}$ and $\overline{MRDC}$ are used instead of ALE from the 8288 to allow sufficient row address setup time to the memory (the row addresses are delayed by two propagation delays, 74LS373, and TMS4500A). This signal is also fed into the input of a 74S74 to be synchronized with the rising edge of CLK (see Figure 5). The output of the 74S74 is then combined with AD0 and $\overline{BHE}$ and $\overline{CAS}$ to form the upper and lower $\overline{CAS}$ signals. Synchronizing ALE of the TMS4500A with CLK ensures data valid at the memory before the falling edge of $\overline{UCAS}$ and $\overline{LCAS}$ (necessary for early write operation). The $\overline{UWR}$ and $\overline{LWR}$ signals are driven by $\overline{AMWC}$ to guarantee them to be valid before $\overline{UCAS}$ and $\overline{LCAS}$ low. $\overline{AMWC}$ is buffered to drive the 32 DRAMs.

This Application Report has illustrated the use of the TMS4500A and TM4164EC4 for a flexible, high-density memory array. The TMS4500A gives the board a static appearance, while the TM4164EC4 provides a density of greater than five memory devices per square inch. Higher densities can be obtained with narrower SIP spacings requiring adequate cooling. The 8086 interface provides a typical application and demonstrates the flexibility of the board. As circuit board designers strive to reduce board space and implement more functions on a board, the use of SIPs such as the TM4164EC4 will provide a vehicle by which this goal can be achieved.

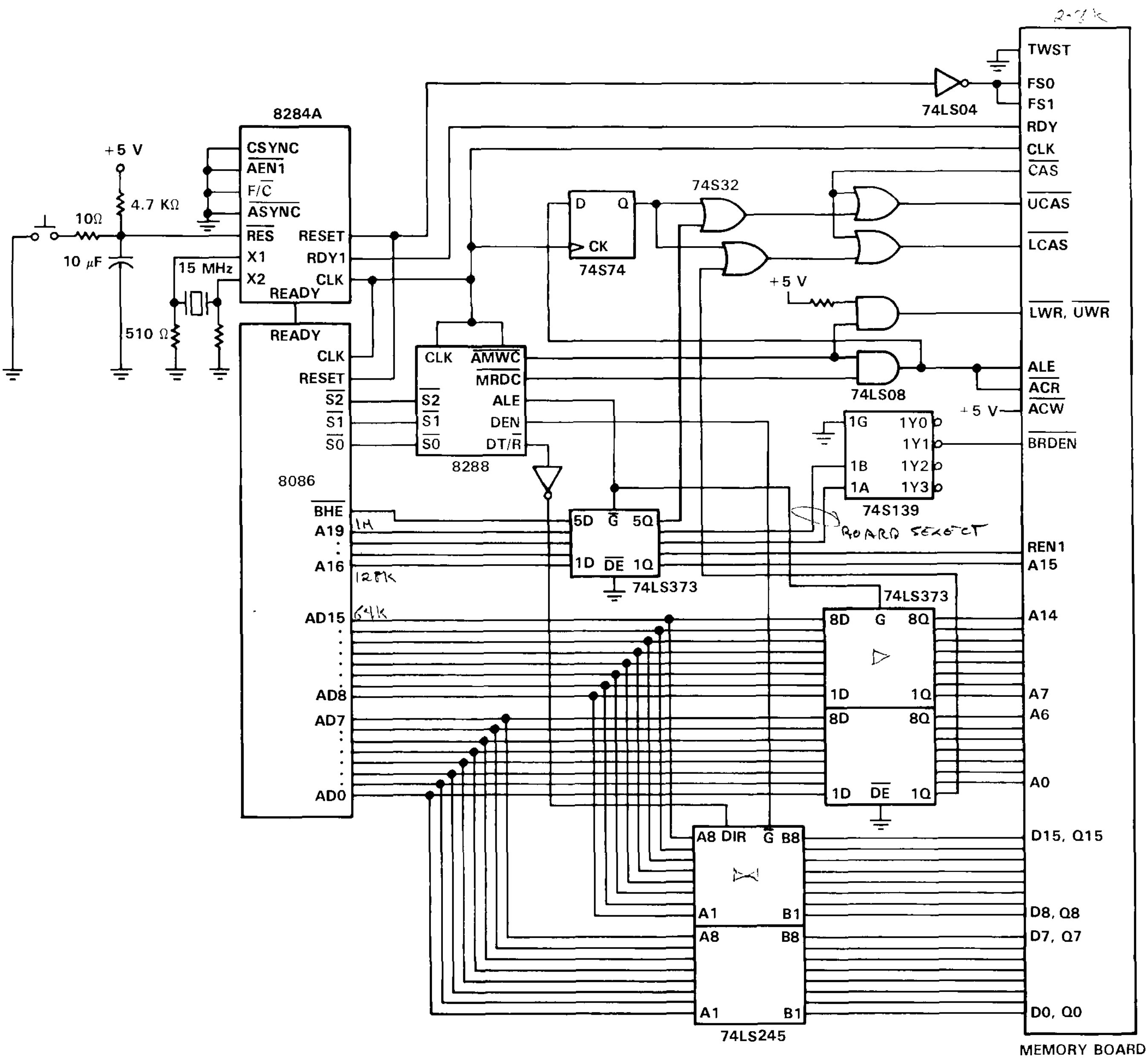

Figure 4. 8086 Interface

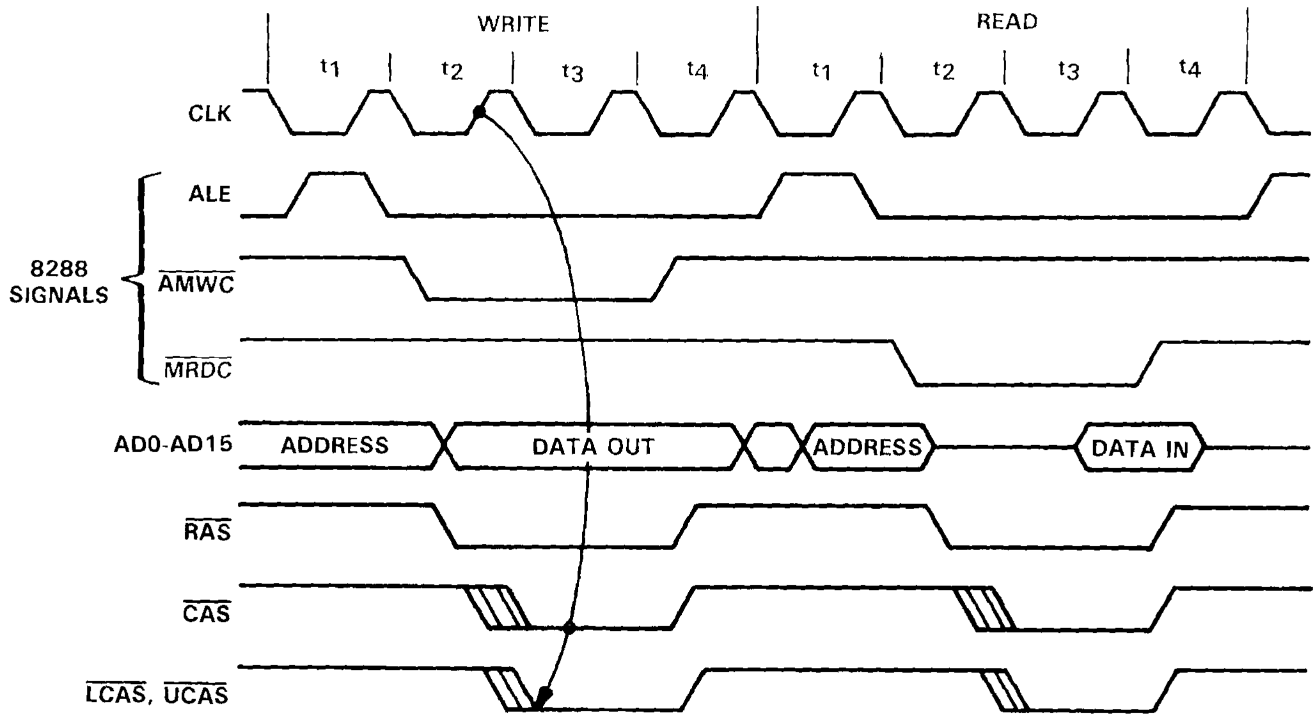

Figure 5. 8086 Interface Timing Diagram

APPENDIX A
TM4164EC4 PIN OUT AND FUNCTIONAL BLOCK DIAGRAM

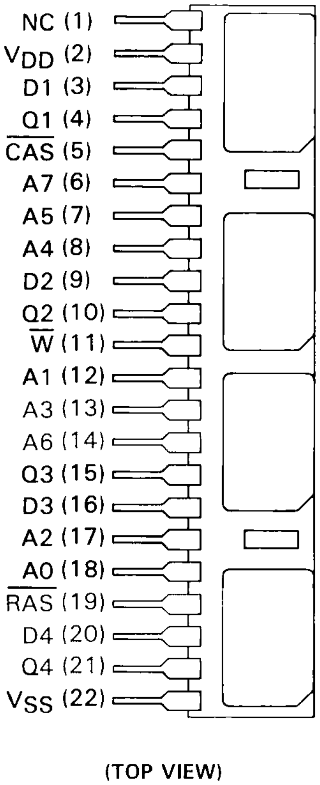

Figure A-1. Pin Out Drawing

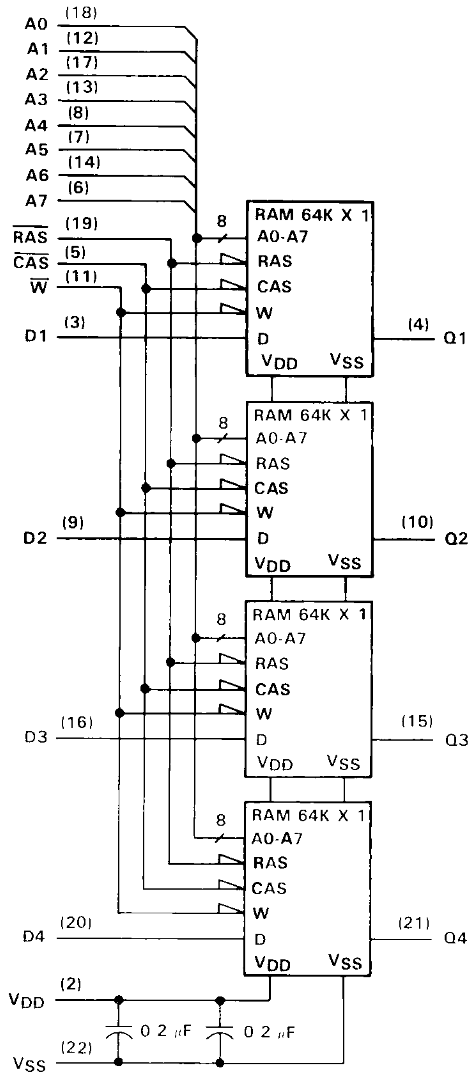

Figure A-2. Functional Block Diagram

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